

FIG. 1A

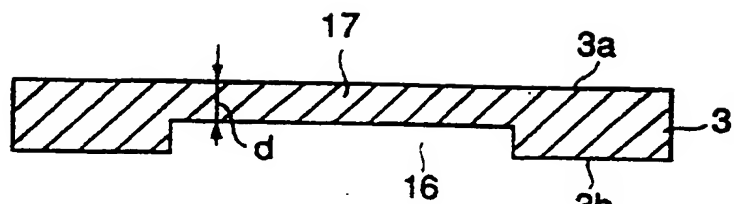


FIG. 1B

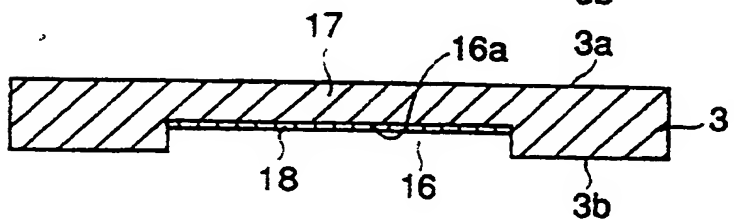


FIG. 1C

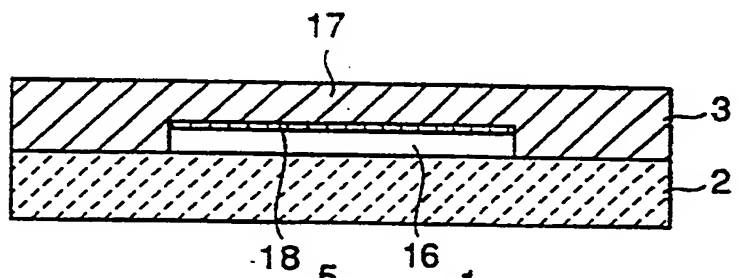


FIG. 1D

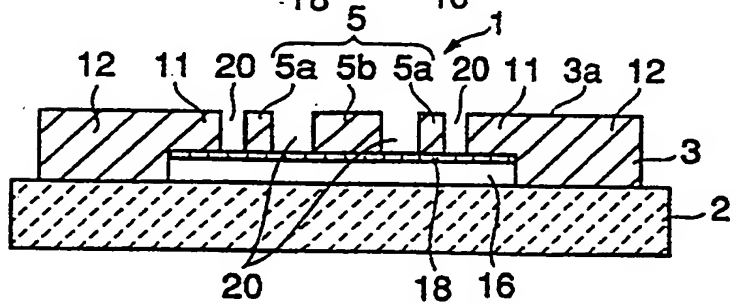
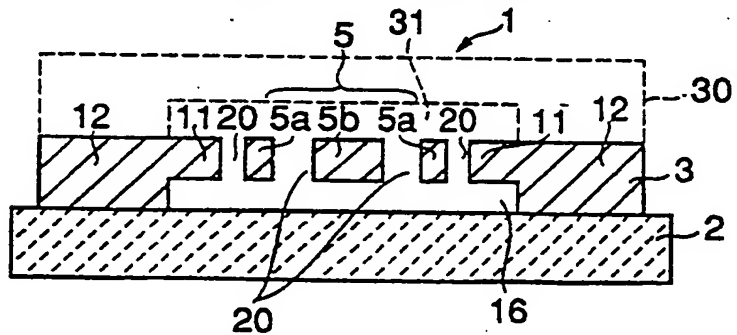


FIG. 1E



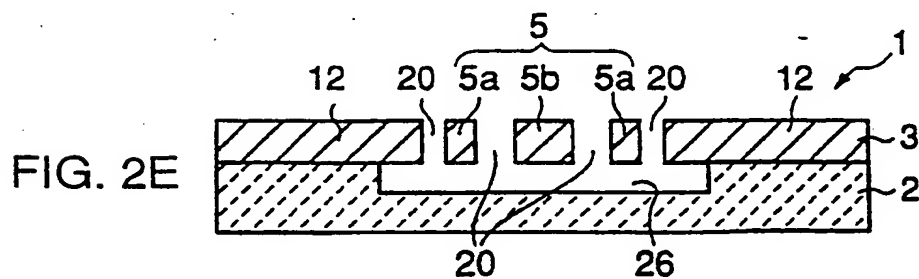
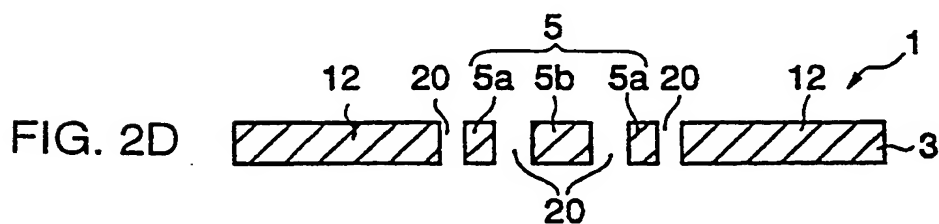
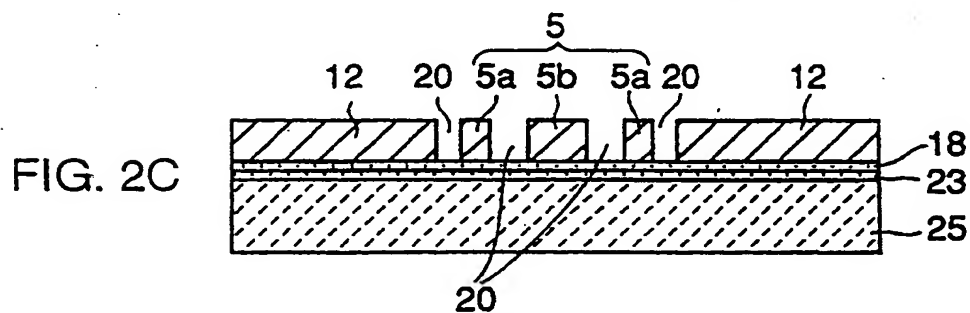
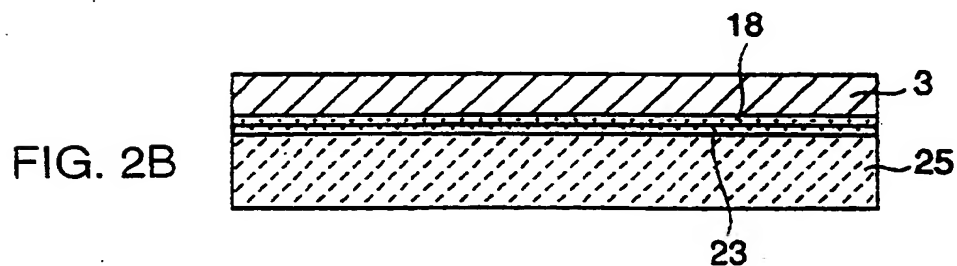
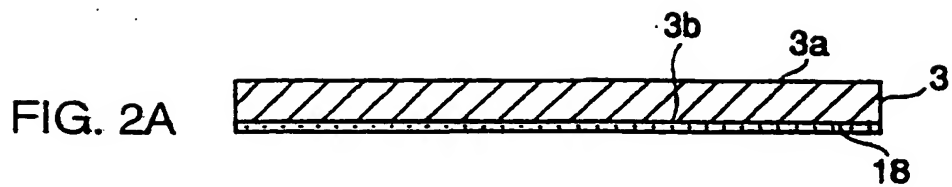


FIG. 3A

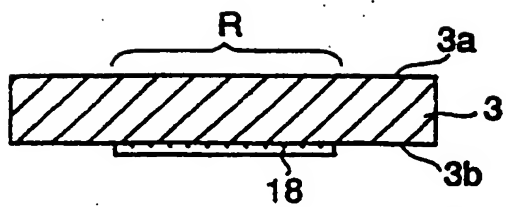


FIG. 3B

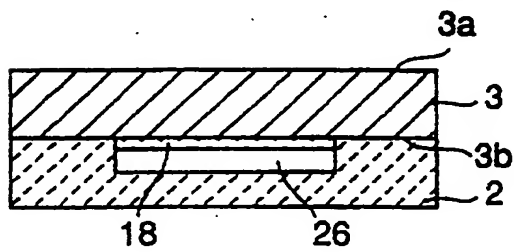


FIG. 3C

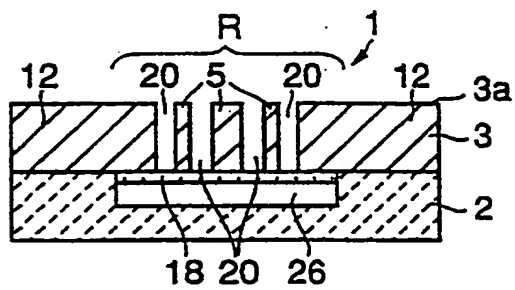


FIG. 3D

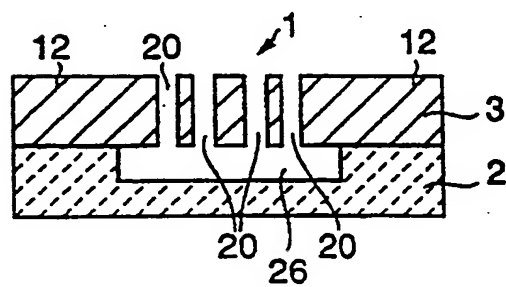


FIG. 4A

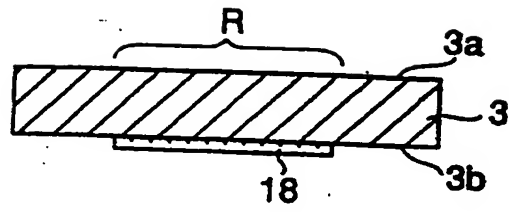


FIG. 4B

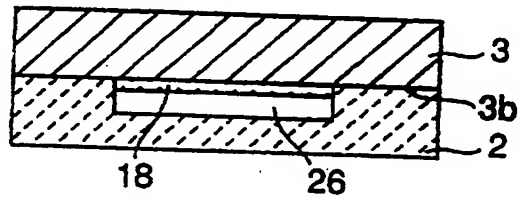


FIG. 4C

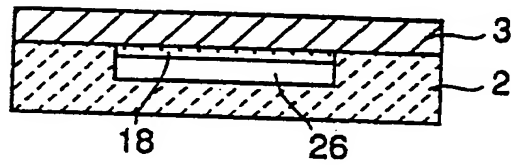


FIG. 4D

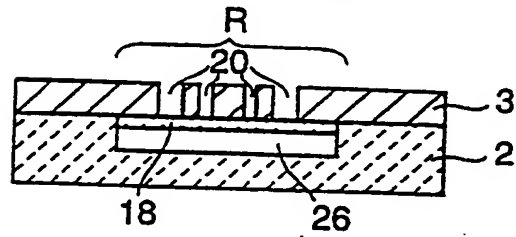


FIG. 4E

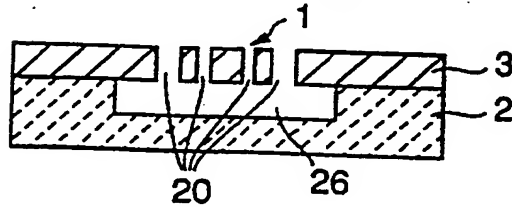


FIG. 5A

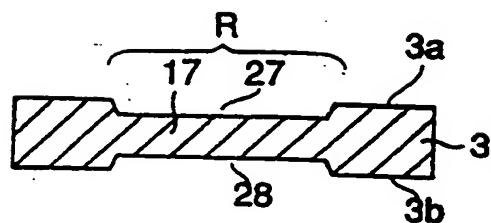


FIG. 5B

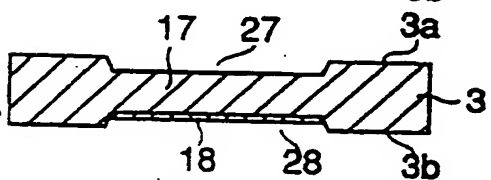


FIG. 5C

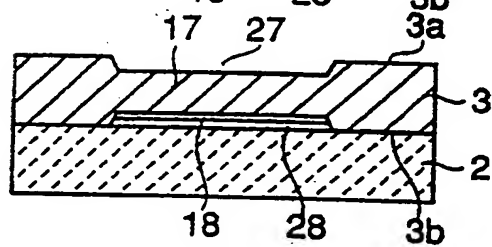


FIG. 5D

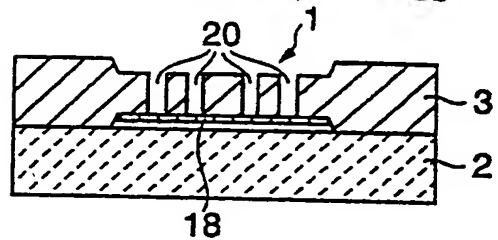


FIG. 5E

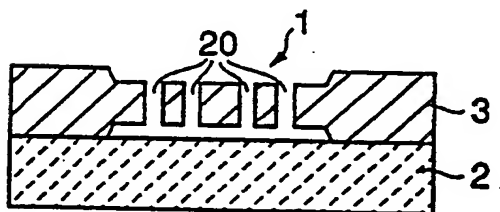


FIG. 6A

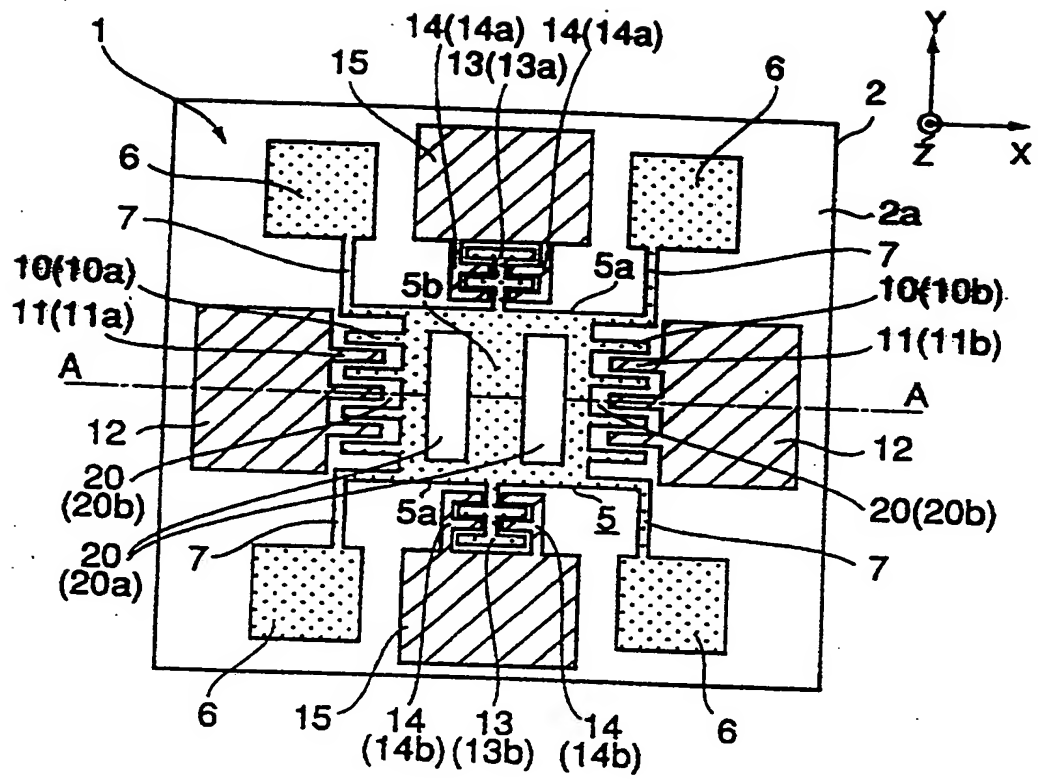
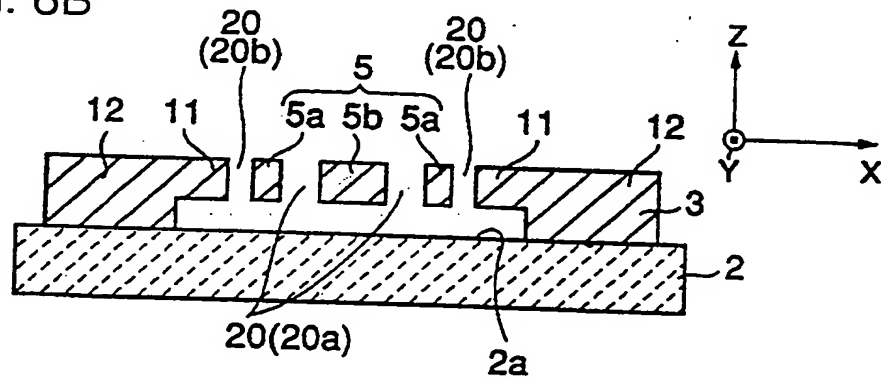


FIG. 6B



This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 3 with a central layer 16. A layer 17 is formed on top of layer 16, with a thickness indicated by 'd'. The layer 17 is wider than the central portion of layer 16, extending over the side regions of the substrate 3.

A cross-sectional view of a substrate 3 with a conductive layer 2. A conductive pad 16 is formed on the conductive layer 2, and a conductive pad 18 is formed on the conductive layer 2.

A cross-sectional diagram of a semiconductor device. It shows a substrate 2 with a dashed diagonal pattern. On top of the substrate is a thin layer 3. Above layer 3 is a patterned layer 5, which consists of three rectangular blocks labeled 5a, 5b, and 5a from left to right. A bracket labeled 5 groups these three blocks. To the left and right of the central blocks are regions labeled 11 and 12. Further out are regions labeled 3a and 12. At the very top, there are labels 1, 10, and 10. Below the substrate 2, there are several curved lines representing electrical connections or fields, labeled with 'n' and '20'. Other labels include 16, 18, and 20 at the bottom.

FIG. 8A  
PRIOR ART

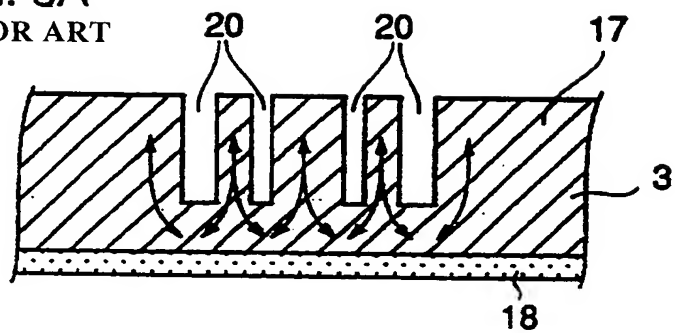


FIG. 8B  
PRIOR ART

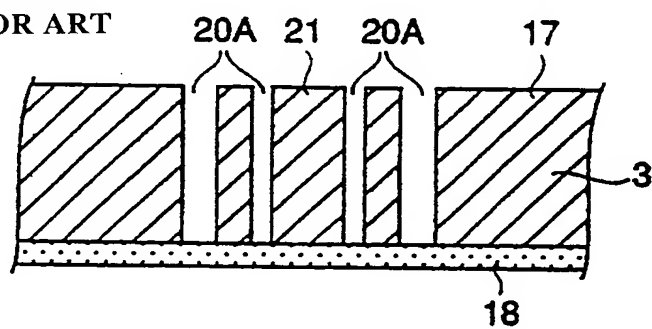


FIG. 8C  
PRIOR ART

